CLAIMS:

1. A multiple chip module, comprising:

a first chip;

a second chip located adjacent to said first chip, wherein said second chip is interconnected with said first chip by one or more orthogonal interconnections; and

a third chip located diagonal to said first chip, wherein said third chip is interconnected with said first chip by one or more diagonal interconnections, wherein said one or more diagonal interconnections between said first chip and said third chip are interconnected between a first set of pins located on said first chip and a second set of pins located on said third chip, wherein a pattern formed by said first set of pins and said second set of pins is a triangular pattern.

2. The multiple chip module as recited in claim 1, wherein a longest diagonal interconnection is substantially a same length as a second longest diagonal interconnection.

3. The multiple chip module as recited in claim 1, wherein a longest diagonal interconnection is substantially a same length as a longest orthogonal interconnection.

4. A method for identifying pin locations to be used for diagonal interconnections in a multi-chip module comprising the steps of:

calculating lengths of a plurality of orthogonal interconnections between a first chip and a second chip, wherein said first chip is located adjacent to said second chip;

calculating lengths of a plurality of diagonal interconnections between said first chip and a third chip, wherein said first chip is located diagonal to said third chip;

receiving an input as to a threshold value, wherein said threshold value is at or below a length of a longest orthogonal interconnection; and

tagging with a first value a first particular number of pins of said first chip used for calculating lengths of diagonal interconnections between said first chip and said third chip that are at or below said threshold value, wherein said first particular number of pins tagged with said first value are used for diagonal interconnections.

5. The method as recited in claim 4, wherein said plurality of diagonal interconnections between said first chip and said third chip are interconnected between a first set of pins located on said first chip and a second set of pins located on said third chip, wherein a pattern formed by said first set of pins and said second set of pins is a triangular pattern.

6. The method as recited in claim 4 further comprising the step of:

tagging with a second value a second particular number of pins of said first chip used for calculating lengths of diagonal interconnections between said first chip and said third chip that are above said threshold value.

7. The method as recited in claim 6, wherein at least a portion of said second particular number of pins tagged with said second value are used for orthogonal interconnections.

8. A computer program product embodied in a machine readable medium for identifying pin locations to be used for diagonal interconnections in a multi-chip module comprising the programming steps of:

calculating lengths of a plurality of orthogonal interconnections between a first chip and a second chip, wherein said first chip is located adjacent to said second chip;

calculating lengths of a plurality of diagonal interconnections between said first chip and a third chip, wherein said first chip is located diagonal to said third chip;

receiving an input as to a threshold value, wherein said threshold value is at or below a length of a longest orthogonal interconnection; and

tagging with a first value a first particular number of pins of said first chip used for calculating lengths of diagonal interconnections between said first chip and said third chip that are at or below said threshold value, wherein said first particular number of pins tagged with said first value are used for diagonal interconnections.

9. The computer program product as recited in claim 8, wherein said plurality of diagonal interconnections between said first chip and said third chip are interconnected between a first set of pins located on said first chip and a second set of pins located on said third chip, wherein a pattern formed by said first set of pins and said second set of pins is a triangular pattern.

10. The computer program product as recited in claim 8 further comprising the programming step of:

tagging with a second value a second particular number of pins of said first chip used for calculating lengths of diagonal interconnections between said first chip and said third chip that are above said threshold value.

11. The computer program product as recited in claim 10, wherein at least a portion of said second particular number of pins tagged with said second value are used for orthogonal interconnections.

12. A system, comprising:

a memory unit operable for storing a computer program operable for identifying pin locations to be used for diagonal interconnections in a multi-chip module;

a processor coupled to said memory unit, wherein said processor, responsive to said computer program, comprises:

circuitry operable for calculating lengths of a plurality of orthogonal interconnections between a first chip and a second chip, wherein said first chip is located adjacent to said second chip;

circuitry operable for calculating lengths of a plurality of diagonal interconnections between said first chip and a third chip, wherein said first chip is located diagonal to said third chip;

circuitry operable for receiving an input as to a threshold value, wherein said threshold value is at or below a length of a longest orthogonal interconnection; and

circuitry operable for tagging with a first value a first particular number of pins of said first chip used for calculating lengths of diagonal interconnections between said first chip and said third chip that are at or below a threshold number, wherein said first particular number of pins tagged with said first value are used for diagonal interconnections.

13. The system as recited in claim 12, wherein said plurality of diagonal interconnections between said first chip and said third chip are interconnected between a first set of pins located on said first chip and a second set of pins located on said third chip, wherein a pattern formed by said first set of pins and said second set of pins is a triangular pattern.

14. The system as recited in claim 12, wherein said processor further comprises:

circuitry operable for tagging with a second value a second particular number of pins of said first chip used for calculating lengths of diagonal interconnections between said first chip and said third chip that are above said threshold value.

15. The system as recited in claim 14, wherein at least a portion of said second particular number of pins tagged with said second value are used for orthogonal interconnections.